Intel® 82566 Layout Checklist (version 1.0)

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Obtain the most recent documentation and specification updates	Documents are subject to frequent change		
	Route the GLCI and MDI differential traces before routing the digital traces.	Layout of differential traces is critical. Refer to the design guide for detailed routing requirements.		
82566	Place the 82566 at least 1 inch from the edge of the board.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately 1 inch behind the magnetics module.		
	Place the RBIAS compensation resistor less than 1 inch from the 82566.			
	Place the KBIAS compensation resistor less than 1 inch from the 82566.			
	Place the JKCLK series resistor within 2 inches of the 82566.	The 33 Ω series resistor is required for signal integrity.		
	Route the JKCLK clock as a 50 Ω single-ended impedance (± 20%).	Controlled impedance is required to reduce ringing and improve signal quality at the ICH.		
	Keep JKCLK at least 7 mils or more away from other traces.	Keep 7 mil spacing to digital traces, I/O ports, and board edge. More spacing might be required to other high speed traces or clocks.		
Clock Source	Place crystal and load capacitors less than 0.75 inches from the 82566.	This reduces EMI.		
	Keep crystal lines 15 mils away from other signals.	This includes spacing to other digital traces, I/O ports, board edge, transformers, and differential pairs.		
	Keep crystal traces 6 mils in width.	6 mils is best for low capacitance, which is important for crystal circuit frequency accuracy.		
LCI Interface	Design traces for 50 Ω single impedance (± 20%).	Check trace impedance with an impedance calculator. Traces are 4 mils wide with 5 mils separation for designs with a dielectric thickness of 2.8 mils (nominal).		

LCI Interface (continued)	JTXD[2:0] and JRXD[2:0] signals are limited to a maximum length of 10 inches for ICH8 and 12 inches for ICH9.	For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces. The length of each JTXD and JRXD trace must be equal in length to the JKCLK trace or up to 0.5 inches shorter than the JKCLK trace. The JKCLK trace must always be the longest trace in the group. If a length longer than 10 inches (12 inches ICH9) for JTXD[2:0] and JRXD[2:0] is needed, contact your Intel representative for assistance.		
	Place LCI termination carefully.	Place the JTXD[2:0] termination close to the ICH. Place the JRXD[2:0] termination close to the 82566.		
MDI Differential Pairs	Design traces for 100 Ω differential impedance (± 20%)	Primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator.		
	Place the 82566 at least 1 inch from the integrated magnetics module but less than 4 inches.	With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board, increasing EMI. If the board does not have power and ground planes along the edge, the problem could be worse. Larger spacing increases the insertion loss of the MDI signals and decreases amplitude, which might cause IEEE failures. The optimum location is approximately 1 inch behind the magnetics module.		
	Avoid highly resistive traces (for example, 4 mil traces longer than 4 inches)	If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces. Traces are 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils (nominal).		
	Make traces symmetrical	Pairs should be matched at pads, vias and turns. Rules for the autorouter should be carefully established. Asymmetry contributes to impedance mismatch. MDI pairs must not use autorouter.		Reference the geometry of the platform design guide.
	Do not make 90° bends.	Bevel corners with turns based on 45° angles		
	Minimize through holes (vias).	If using through holes (vias), the budget is two 10 mil finished hole size vias per trace.		
	Keep trace-to-trace length difference within each pair to less than 50 mils.	This minimizes signal skew and common mode noise. Improves long cable performance.		
	Pair-to-pair trace length does not have to be matched as differences are not critical.	The difference between the length of longest pair and the length of the shortest pair should be approximately 2 inches. A 25% difference in length from the longest pair to the shortest pair is typical.		
	Keep differential pairs 30 mils or more away from each other and away from parallel digital traces.	This minimizes crosstalk and noise injection. Guard traces are generally not recommended and can reduce the impedance if done incorrectly.		

MDI Differential Pairs (continued)	Keep traces at least 0.1 inches away from the board edge.	This reduces EMI.		
	Avoid unused pads and stubs along the traces	Unused pads and stubs cause impedance discontinuities.		
	Route traces on appropriate layers.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the GND planes. When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias. If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling capacitor on the power and ground within 40 mils of the signal vias. Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality. Make sure digital signals on adjacent layers cross at 90° angles.		
	Place MDI termination resistors and capacitors less than 0.25 inches from the 82566.	Improves IEEE performance by reducing reflections. Use symmetrical pads. Minimize any stubs.		
Magnetics Module	Capacitors connected to center taps should be placed very close (less than 0.1 inch recommended) to integrated magnetics module.	Placement contributes directly to IEEE performance.		
	Deliver 1.8V to the magnetic center tap with a plane.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum). Planes are lower inductance and lower resistance than traces and provide better IEEE performance.		
GLCI Interface	Design traces for 100 Ω differential impedance (± 20%)	Paired 50 Ω traces do not make 100 Ω differential. Check impedance calculator. Traces are 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils (nominal).		
	Long traces are allowed up to 13 inches, but avoid highly resistive traces.	For long distances, thick traces are preferred over wide traces. Modify board stackup if necessary to avoid highly resistive traces. Traces should be routed diagonal to the FR4 weave to maintain consistent impedance. If 1 ounce copper is used, minimum trace spacing within each differential pair must be >= 8 mils. GLCI trace lengths can be extended up to 13 inches by limiting the number of vias in the TX and RX paths of the GLCI traces to 4.		
	Make traces symmetrical.	Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch.		
	Do not make 90° bends.	Bevel corners with turns based on 45° angles.		

GLCI Interface (continued)	Minimize through holes (vias).	If using through holes (vias), the budget is six 10 mil finished hole size vias on the Rx traces, and 4 on the Tx traces. The Rx side vias must be reduced to 4 inches in order to increase the length of the GLCI buses to 13 inches.		
	Keep traces close together within differential pairs.	Traces are 4 mils wide with 8 mils of separation (inside of a pair) for designs with a dielectric thickness of 2.8 mils (nominal). If spacing is less than 6 mils, it is almost impossible to achieve >90 Ω differential impedance.		
	Keep trace-to-trace length difference within each pair to less than 10 mils.	Minimizes signal skew and reduces common mode conversion.		
	Keep GLCI differential pairs approximately 15 mils or greater away from each other.	The minimum separation is 15 mils for designs with a dielectric thickness of 2.8 mils (nominal). Minimizes crosstalk and noise injection. This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs. If using a larger dielectric thickness, keep adjacent traces away by at least 6 times the dielectric thickness. For example, 4.5 mil thick FR4; spacing >= 27 mils.		
	Keep traces greater than 0.1 inch from the board edge.	Reduces EMI.		
	Avoid unused pads and stubs along the traces.	Use 0 Ω resistors sparingly if needed.		
	Route traces on appropriate layers always reference to GND.	Run pairs on different layers as needed to improve routing. Use layers adjacent to ground layers. There must be no splits in the GND planes. When differential signals transition from one board layer to another, place ground vias within 40 mils of the signal vias. If the differential signals transition from a ground referenced layer to a power referenced layer, place a decoupling cap on the power and ground within 40 mils of the signal vias. Avoid broadside coupling to traces on other layers. The broadside effect significantly increases the insertion loss and reduces signal quality. Make sure digital signals on adjacent layers cross at 90° angles.		
	For the GLCI interface, place AC coupling capacitors close to the transmitters.	The AC coupling is always at the transmitter on the GLCI interface.		
Power Supply and Signal Ground	Keep the routed length of the CTRL_10 and CTRL_18 signals to the external PNP transistors less than 1 inch.	This reduces oscillation and ripple in the power supply.		
	Route the CTRL_10 and CTRL_18 signals as 12 mil wide traces.	Low inductance and low capacitance feedback paths reduce oscillations and ripple in the power supply.		
	Keep CTRL_10 and CTRL_18 lines greater than 10 mils away from other signals.	This includes spacing to other digital traces, I/O ports, board edge, transformers and differential pairs.		

Power Supply and Signal Ground (continued)	Use planes to deliver power.	Narrow finger-like planes and very wide traces are allowed. If using traces, aim for 100 mils (minimum). Planes are lower inductance and lower resistance than traces.		
	Use decoupling and bulk capacitors generously.	Place decoupling and bulk capacitors close to the 82566, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends.		
	Verify that the PNP transistors have a 1/2 inch x 1/2 inch thermal relief plane on layer 1.	The extra copper on layer 1 reduces the Theta-ja of the transistor, which improves the power dissipation. Shape is not important, but surface area is important. Connect the thermal relief to the ground plane with 5 vias to minimize the inductance in the power delivery circuit. 82566 IVRd: Apply to both the 1.0V and the 1.8V external PNP transistors. 82566 IVRi: Applies to the 1.8V external PNP transistor. The 1.0V external PNP transistor is not present.		
Chassis Ground	Consider using a separate chassis ground for the LAN connector.	If using a discrete magnetics module, provide a separate chassis ground “island” to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. Split in ground plane should be at least 50 mils wide. Split should run under center of magnetics module. Differential pairs never cross the split. If using an integrated magnetics module without USB, provide a separate chassis ground “island” to ground around the RJ-45 connector. Split in ground plane should be at least 50 mils wide. If using an integrated magnetics module with USB, do not use a separate chassis ground		
	Consider placing ground stitching capacitors.	If using an integrated magnetics module without USB, place 4-6 pairs of pads for “stitching” capacitors to bridge the gap from chassis ground to signal ground. Determine exact number and values empirically based on EMI performance. Expect to populate approximately two capacitor sites. If using an integrated magnetics module with USB, do not use stitching capacitors.		
LED Circuits	Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI.		

LED Circuits (continued)	If using decoupling capacitors on LED lines, place them carefully.	Capacitors on LED lines should be placed near the LEDs (typically adjacent to integrated magnetics module).		